REMARKS

Receipt of the final Office Action of January 25, 2007 is hereby acknowledged. In that action the Examiner: 1) rejected claim 1 as allegedly unpatentable over Park (U.S. Pat. No. 6,832,305) in view of So (U.S. Pat. No. 6,944,746); 2) rejected claims 2-4 and 7 as allegedly unpatentable over Park in view of So in further view of Seal (U.S. Pat. No. 6,965,984); 3) rejected claims 5-6 and 8 as allegedly unpatentable over Park in view of So in further view of Gorishek (U.S. Pat. No. 6,308,255); 4) rejected claims 9-20 as allegedly unpatentable over Park in view of Gorishek in further view of So; 5) rejected claims 21-26 as allegedly unpatentable over Park in view of So in further view of Gorishek; and 6) rejected claims 27-33 as allegedly unpatentable over Park in view of So in further view of Gorishek.

With this Preliminary Amendment, Applicants amend claims 1, 5-9, 11-12, 14-15, 17-18, 20-21, 25-27, and 31-32. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. ART-BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly unpatentable over Park in view of So. Applicants amend claim 1 to more clearly distinguish over Park's single mode decoders, to remove "adapted to" terminology, and to replace "permanently" terminology. The amendment finds support in the original specification at Paragraphs [0020], [0021], [0026], [0028], [0032], and [0033], and Figure 2 (element 162), Figure 3 (element 162), Figure 4 (element 162 and element 152), and Figure 5 (element 162 and element 152).

Park is directed to method and apparatus for executing co-processor instructions (Park Title). In particular and in relevant part, Park appears to disclose a main processor which decodes main processor instructions and a co-processor which decodes co-processor instructions, where the main and co-processor instructions are from the same instruction set (See Park Col. 3, lines 38-67 and Col. 4, lines 1-48). Park discloses that in the absence of the co-processor, the main processor will perform the decoding functions, and the co-processor is used primarily to increase processing speed (See Park Col. 1, lines 22-24). In Park's main processor/co-processor scheme, the main processor only

decodes main processor instructions without indication as to a particular decoding "mode", and the co-processor only decodes co-processor instructions without indication as to a particular decoding "mode" (Park Col. 4, lines 1-4 and Col. 4, lines 22-24). Park further discloses an instruction type code that is used to distinguish main processor instructions from co-processor instructions within the single instruction set (Park Col. 3, lines 55-57, Col. 4, lines 2-3, and Col. 4, lines 64-65). Thus, Park teaches a main processor and a co-processor, which separately decode main processor instructions and co-processor instructions belonging to **the same instruction set**, without indication as to a particular decoding "mode". So is directed to RISC processor supporting one or more uninterruptible co-processors (So Title). The Office Action has relied on So only for a teaching of a single decoder.

Claim 1, by contrast, specifically recites, "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the processor comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**". Applicants respectfully submit that Park and So do not teach or fairly suggest such a system. As the Examiner is no doubt aware, there is no indication that Park's main processor instructions and co-processor instructions are from different instruction sets. The Office Action relies merely on Park's teaching of the existence of main processor instructions and co-processor instructions in alleging that Park discloses two instruction sets. This reliance is misplaced. Park's disclosure that a complete co-processor instruction comprises most significant bits (MSBs) from the main program memory and least significant bits (LSBs) from the co-processor program memory, and that a complete main processor instruction comprises only those MSBs that are also sent to the co-processor, suggests that Park's system employs a single instruction set architecture. Thus, Park's disclosure of main processor instructions and co-processor instructions does not refer to different instruction sets, but rather to different bit width instructions that are decoded by either the main processor or the co-processor.

As the Examiner is no doubt aware, there is also no indication that that the decoding "mode" varies between Park's main processor decoder and co-processor decoder. The Office Action relies on Park's teaching of two decoders, a main processor decoder which decodes main processor instructions and a co-processor decoder which decodes co-processor instructions, in alleging that each decoder is decoding in one of two distinct modes. This reliance is misplaced. Even considering together the decoding of main processor instructions by the main processor and the decoding of co-processor instructions by the co-processor, Park still does not disclose two "modes" of operation. Furthermore, none of the instruction type code, the main processor, or the co-processor has a flag that indicates decoding in a particular "mode". In particular, the instruction type code only distinguishes main processor instructions from co-processor instructions within the single instruction set and does not indicate or change a decoding mode of either the main processor decoder or the co-processor decoder as disclosed by Park. In fact, Park does not disclose any type of flag to indicate that instructions are being decoded in one of two modes.

Thus, even if the teachings of So are precisely as the Office Action suggests (which Applicants do not admit), Park and So still do not teach, and in fact appear to teach away from, a system having "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the processor comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**".

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-8), should be allowed. Applicants amend claims 5-8 to replace "permanently" terminology. No new matter is added.

B. Claim 9

Claim 9 stands rejected as allegedly unpatentable over Park in view of Gorishek in further view of So. Applicants amend claim 9 to more clearly distinguish over Park's single mode decoders, to correct antecedent basis shortcomings, and to replace

"permanently" terminology. The amendment finds support in the original specification at Paragraphs [0020], [0021], [0026], [0028], [0032], and [0033], and Figure 2 (element 162), Figure 3 (element 162), Figure 4 (element 162 and element 152), and Figure 5 (element 162 and element 152).

Park teaches a main processor and a co-processor, which separately decode main processor instructions and co-processor instructions belonging to the same instruction set, without indication as to a particular decoding "mode". Gorishek is directed to symmetrical multiprocessing bus and chipset used for coprocessor support allowing non-native code to run in a system (Gorishek Title). The Office Action relies on Gorishek only for a teaching of switching the decoding permanently from one mode to another. So is directed to RISC processor supporting one or more uninterruptible co-processors (So Title). The Office Action has relied on So only for a teaching of a single decoder.

Claim 9, by contrast, specifically recites, "decoding instructions from **the first instruction set in a first mode** and decoding instructions from **the second instruction set in a second mode**", and "wherein **a status register** is configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode.**" Applicants respectfully submit that Park, Gorishek, and So do not teach or fairly suggest such a system. In particular, the Office Action unduly relies on Park's teaching of the existence of main processor instructions and co-processor instructions in alleging that Park discloses two instruction sets, and the Office Action unduly relies on Park's teaching of two decoders, a main processor decoder which decodes main processor instructions and a co-processor decoder which decodes co-processor instructions, in alleging that each decoder is decoding in one of two distinct modes. Thus, even if the teachings of Gorishek and So are precisely as the Office Action suggests (which Applicants do not admit), Park, Gorishek, and So still do not teach, and in fact appear to teach away from, "decoding instructions from **the first instruction set in a first mode** and decoding instructions from **the second instruction set in a second mode**", and "wherein **a status register** is configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode.**"

Based on the foregoing, Applicants respectfully submits that claim 9, and all claims which depend from claim 9 (claims 10-20), should be allowed. Applicants amend claims 11-12, 14-15, 17-18, and 20 to remove "step of" terminology and to replace "permanently" terminology. No new matter is added.

C. Claim 21

Claim 21 stands rejected as allegedly unpatentable over Park in view of So in further view of Gorishek. Applicants amend claim 21 to more clearly distinguish over Park's single mode decoders and to remove "adapted to" terminology. The amendment finds support in the original specification at Paragraphs [0020], [0021], [0026], [0028], [0032], and [0033], and Figure 2 (element 162), Figure 3 (element 162), Figure 4 (element 162 and element 152), and Figure 5 (element 162 and element 152).

Park teaches a main processor and a co-processor, which separately decode main processor instructions and co-processor instructions belonging to the same instruction set, without indication as to a particular decoding "mode". The Office Action has relied on So only for a teaching of a single decoder. The Office Action has relied on Gorishek only for a teaching of switching the decoding permanently from one mode to another.

Claim 21, by contrast, specifically recites, "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the processor comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**". Applicants respectfully submit that Park, So, and Gorishek do not teach or fairly suggest such a system. In particular, the Office Action unduly relies on Park's teaching of the existence of main processor instructions and co-processor instructions in alleging that Park discloses two instruction sets, and the Office Action unduly relies on Park's teaching of two decoders, a main processor decoder which decodes main processor instructions and a co-processor decoder which decodes co-processor instructions, in alleging that each decoder is decoding in one of two distinct modes. Thus, even if the teachings of So and Gorishek are precisely as the Office Action suggests (which Applicants do not admit), Park, So, and

Gorishek still do not teach, and in fact appear to teach away from, "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from a **second instruction set in a second mode**", and "wherein the processor comprises a **status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**".

Based on the foregoing, Applicants respectfully submit that claim 21, and all claims which depend from claim 21 (claims 22-26), should be allowed. Applicants amend claims 25-26 to replace "permanently" terminology. No new matter is added.

D. Claim 27

Claim 27 stands rejected as allegedly unpatentable over Park in view of So in further view of Gorishek. Applicants amend claim 27 to more clearly distinguish over Park's single mode decoders and to remove "adapted to" terminology. The amendment finds support in the original specification at Paragraphs [0020], [0021], [0026], [0028], [0032], and [0033], and Figure 2 (element 162), Figure 3 (element 162), Figure 4 (element 162 and element 152), and Figure 5 (element 162 and element 152).

Park teaches a main processor and a co-processor, which separately decode main processor instructions and co-processor instructions belonging to the same instruction set, without indication as to a particular decoding "mode". The Office Action has relied on So only for a teaching of a single decoder. The Office Action has relied on Gorishek only for a teaching of switching the decoding permanently from one mode to another.

Claim 27, by contrast, specifically recites, "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the system comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**". Applicants respectfully submit that Park, So, and Gorishek do not teach or fairly suggest such a system. In particular, the Office Action unduly relies on Park's teaching of the existence of main processor instructions and co-processor instructions in alleging that Park discloses two instruction sets, and the Office Action unduly relies on Park's teaching of two decoders, a main

processor decoder which decodes main processor instructions and a co-processor decoder which decodes co-processor instructions, in alleging that each decoder is decoding in one of two distinct modes. Thus, even if the teachings of So and Gorishek are precisely as the Office Action suggests (which Applicants do not admit), Park, So, and Gorishek still do not teach, and in fact appear to teach away from, "decode logic configured to decode instructions from **a first instruction set in a first mode** and configured to decode instructions from **a second instruction set in a second mode**", and "wherein the system comprises **a status register** configured to indicate whether the decode logic is decoding instructions in the **first mode** or the **second mode**".

Based on the foregoing, Applicants respectfully submit that claim 27, and all claims which depend from claim 27 (claims 28-33), should be allowed. Applicants amend claims 31-31 to replace "permanently" terminology. No new matter is added.

II. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees

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required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

Michael E. Ramon
PTO Reg. No. 52,147
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9181 (Fax)
Agent for Applicants